

REMARKS

This application has been reviewed in light of the Office Action dated May 16, 2006. Claims 1-19 and 29 are pending in the application. By the present amendment, claims 1 and 10 have been amended. No new matter has been added. The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested.

By the Office Action, claims 1 and 10 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

The Examiner stated that “to determine actions to remedy problems prior to completing fabrication of integrated circuits on the integrated circuit substrate” in claims 1 and 10 and “partially fabricated” in claim 10 are not mentioned in the specification. The Applicants respectfully disagree.

Page 2 of the Summary recites: “Measurements are taken to provide feedback for in-situ adjustments to circuit parameters and responses.”

The first paragraph of the Detailed Description recites: “Exemplary embodiments measure key process parameters manifested as circuit performance in a contactless manner. These measurements may be particularly useful in a semiconductor fabrication process if they are made at a sufficiently early point in the process flow. In this way, the measurement information may be used to “adaptively” alter the subsequent steps in wafer fabrication to compensate for any measured discrepancies between measured and desired wafer parametrics.”

The last paragraph on page 6, recites: “In particularly useful embodiments, the data from in-situ measurements could be fed into a database, and analyzed so that adaptations could be made to either downstream process parameters or to select from one of a set of mask plate combinations that would implement wiring changes that effect the compensation desired. This

procedure could be seamlessly incorporated into the control flow of a fabrication plant with minimal additional cost. The largest cost may be represented by additional mask plates that represent possible process options. In addition, if it is found that the parameters are beyond recovery, the wafers can also be scrapped at an earlier point in the process, thereby saving the expense of further processing on wafers that eventually would be scrapped.”

See also block 206 in FIG. 5.

These are but some of the examples that support the claim language of claims 1 and 10. It is respectfully noted that according to MPEP 2163.02: The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.

Claims 1 and 10 have been amended in a way believed to provide further clarity in the event that the claims were misinterpreted by the Examiner.

It is clear from the above citations that the inventor had possession of the invention, as set forth in the amended claims. Reconsideration is earnestly solicited.

By the Office Action, the drawings were objected to for not showing every feature in the claims. The Examiner stated that “a test device including the source” recited in claim 10 was not shown in the drawings.

The test device may include a probe ring 23 that supports a membrane 22. The membrane 22 is placed in close proximity without contact with the wafer 10 to enhance the coupling coefficient between the coils of a transformer or a plate of a capacitor (energy sources). FIG. 4B shows a pad 40 of a capacitor (or transformer coil) (this is a source) on a test device 23. Therefore, a test device including a source is clearly depicted in at least FIG. 4B.

Reconsideration is earnestly solicited.

By the Office Action, claims 1-2, 4, 7-10, 15-16 and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,759,863 to Moore (hereinafter Moore) in view of U.S. Patent No. 5,556,029 to Min et al. (hereinafter Min).

The Applicants respectfully disagree with the rejection.

Moore is directed to a test system that includes a test circuit that communicates with an off chip test unit by using RF signals. An antenna in the test circuit powers the test circuit which tests the actual chips themselves. No alignment between the test circuits and the test unit is needed to conduct communications since wireless communications are carried out.

The Examiner stated: Moore fails to disclose “components that mirror behavior on the integrated circuit”. Moore also fails to disclose or suggest “the source does not make physical contact with the integrated circuit substrate to transfer power to the measurement circuit when the source is in alignment with the power transfer component”.

Min fails to cure these deficiencies. The system of Min is designed to induce current flow in a semiconductor junction using a pulsed beam. While the pulsed beam may be considered an energy source, the beam energizes only specific optically sensitive components. Other portions of the chip cannot be measured and the devices tested must be completely fabricated. There is no disclosure or suggestion of in-situ tests that provide data on a partially fabricated semiconductor chip.

In addition, there is no test or measurement circuit as set forth in the present claims. Furthermore, Min actually contacts the wafer in order to measure current flow (see e.g., Title “Pulsed Single Contact Optical Beam Current Analysis of Integrated Circuits”). This is in direct opposition of the teachings of the present invention. In Min, a single contact 55 is made to the device and another contact 66 connects to ground (and to the wafer). Each time a different

device or chip is tested this contact needs to move to another location. One skilled in the art reading Min would not be led to combine its teachings with Moore to arrive at the present invention. The present invention is directed to a system that avoids physical contact with the wafer yet still provides energy to test components. Min teaches making contact with a wafer to induce current flow and then optically images the current flow to test a junction.

Even if, *arguendo*, it is proper to combine Moore with Min, the cited combination fails to disclose or suggest all of the claim elements. Claim 1 now includes, *inter alia*, a system for measuring circuits on an integrated circuit substrate during fabrication, including ... [a] measurement circuit comprising a power transfer device including a power transfer component, which receives energy from a source where the source does not make physical contact with the integrated circuit substrate to transfer power to the measurement circuit when the source is in alignment with the power transfer component, the measurement circuit including components that mirror behavior of the integrated circuit so that process parameters are measured for the components to provide information about processing steps and provide information for determining actions to remedy problems prior to completing fabrication of integrated circuits on the integrated circuit substrate.

The cited combined fails to disclose or suggest at least: (1) measurement circuit ... which receives energy from a source where the source does not make physical contact with the integrated circuit substrate to transfer power to the measurement circuit when the source is in alignment with the power transfer component, and (2) the measurement circuit including components that mirror behavior of the integrated circuit so that process parameters are measured for the components to provide information about processing steps and provide information for determining actions to remedy problems prior to completing fabrication of integrated circuits on

the integrated circuit substrate.

Moore discloses an RF system where alignment of the energy source is not needed. Further, Moore fails to disclose or suggest employing components in the measurement circuit that mirror behavior of the integrated circuit, and instead provides test circuits throughout the wafer to permit “100%” testing (col. 6 line 36-40) of all of the actual IC chips (see FIG. 4). This leads to additional expense and the use of chip real estate.

Min also fails to disclose or suggest components in the measurement circuit that mirror behavior of the integrated circuit, therefore fails to cure the deficiencies of Moore. The Examiner stated that Min teaches components in the measurement circuit that mirror behavior of the integrated circuit at col. 2 line 45-46. Upon reviewing Min, the Applicant finds no teaching or suggestion of components in the measurement circuit that mirror behavior of the integrated circuit. Min does not even provide an on-chip measurement circuit.

Further, the Examiner states the motivation for combining Min and Moore includes the expected advantage of testing the integrated circuit without the need for probing an interior portion of the circuit as disclosed by Min. While Min reduces probing individual components, Min fails to eliminate contactless testing since Min continues to make physical connections with the wafer and chips (See FIG. 2, contact 55).

In addition, while Min teaches that an optical beam must be incident on a junction, Min fails to disclose or suggest that the source is in alignment with the power transfer component of a measurement circuit.

The arguments set forth above are equally applicable to claim 10 which includes similar recitations.

Since Moore and/or Min fail to disclose or suggest all elements of the present invention,

claims 1 and 10 are believed to be in condition for allowance for at least the reasons stated.

Claims dependent from claims 1 and 10 are also believed to be in condition for allowance at least due to their dependencies from claims 1 and 10. The dependent claims are believed to be allowable for other reasons as well.

By the Office Action, claims 3, and 11 stand rejected under 35 U.S.C. §103(a) as being anticipated by Moore in view of Min and further in view of U.S. Patent No. 6,787,801 to Fischer et al. (hereinafter Fischer).

The Applicant respectfully disagrees with the rejection since Fischer fails to cure the deficiencies of Moore and Min as set forth above. Claims 3 and 11 are therefore believed to be in condition for allowance for at least the above mentioned reasons. Reconsideration is respectfully requested.

By the Office Action, claims 5 and 13 stand rejected under 35 U.S.C. §103(a) as being anticipated by Moore in view of Min and further in view of U.S. Patent No. 6,686,760 to Hirt (hereinafter Hirt).

The Applicant respectfully disagrees with the rejection since Hirt fails to cure the deficiencies of Moore and Min as set forth above. Claims 5 and 13 are therefore believed to be in condition for allowance for at least the above mentioned reasons. Reconsideration is respectfully requested.

By the Office Action, claims 6 and 14 stand rejected under 35 U.S.C. §103(a) as being anticipated by Moore in view of Min and Hirt and further in view of U.S. Patent Application No. 2002/0047722 to Cook et al. (hereinafter Cook).

The Applicant respectfully disagrees with the rejection since Cook fails to cure the deficiencies of Moore, Min and Hirt as set forth above. Claims 6 and 14 are therefore believed to

be in condition for allowance for at least the above mentioned reasons. Reconsideration is respectfully requested.

By the Office Action, claims 17-18 and 29 stand rejected under 35 U.S.C. §103(a) as being anticipated by Moore in view of Min and further in view of U.S. Patent No. 5,583,445 to Mullen (hereinafter Mullen).

Claim 17 recites that the test device includes a thin film dielectric membrane having the source mounted thereon, and claim 18 recites that the test device includes a probe ring. Claim 29 recites that the thin film dielectric membrane is transparent so that the source mounted thereon can be visually aligned to the power transfer component.

The Examiner cites Mullen to show a membrane probe. However, the membrane probe includes contacts which are directly connected to contact pads for testing a circuit. The contact membrane probe effectively teaches away from the present claims since the membrane is employed to provide physical slack in making an actual connection with the tested device. Therefore, no motivation exists to combine Mullen with Moore and/or Min.

In addition, Mullen fails to cure the deficiencies of Moore and Min. Claims 17-18 and 29 are therefore believed to be in condition for allowance for at least the stated reasons. Reconsideration of the rejection is earnestly solicited.

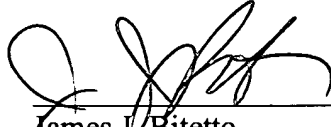
In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested. The Examiner is invited to contact the undersigned to discuss any remaining issues. A telephone conference is believed to be beneficial to advance prosecution of this case.

It is believed that no additional fees or charges are currently due. However, in the event

that any additional fees or charges are required at this time in connection with the application,
they may be charged to applicant's IBM Deposit Account No. 50-0510.

Respectfully submitted,

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By: 
James J. Bitetto
Registration No. 40,513

Mailing Address:

KEUSEY, TUTUNJIAN & BITETTO, P.C.
20 Crossways Park North, Suite 210
Woodbury, NY 11797
Tel: (516) 496-3868
Fax: (516) 496-3869